Memo

To:
From: Hans Manhaeve
CC:
Date:
Concerns: The quest for 0ppm – Training class description

Preamble

The "Quest for 0ppm" training class is fitting into a 0ppm target program and is intended for Project Managers, Design engineers and Test engineers.
To achieve a 0ppm objective in a cost effective way, a proper understanding of the different aspects that make up the product development flow, looked at from both the design and test perspective, is mandatory. An equally important factor is the establishment of a proper interaction between the design and test teams. To achieve these goals the design teams need to be informed about the test capabilities and limitations, enabling the proper introduction of design-for-test methodologies and the fruitful execution of test preparation tasks, the test teams and project managers need to be made aware of the impact of certain design-for-test strategies on the design work and all need to be made aware of the impact of certain design-for-test and test preparation actions on the ability to optimize the test and overall product flow.

Increasing quality demands require a close interaction between the Design & Test departments to reach 0ppm product quality levels. This requires a proper understanding of the test capabilities and limitations as well as a proper understanding of the DFT measures that can be taken. The objective of this training class is to provide the proper knowledge that enables to bridge the gap between Design and Test and to provide a better understanding of the factors involved in reaching a 0ppm quality level.

Training class content

The training class addresses the following topics.

Following an introduction to the 0ppm program, a global situation of the test problem and the need for test is given. The training class is built around three main topic areas. The first one is the Test perspective, the second bridges Design and Test by focussing on the test preparation activities and the third addresses the Design perspective and focuses on design-for-test implementation and application. Before approaching final conclusions test optimization and a number of case studies will be reviewed.

The objective of the "Test perspective" section is to provide a deeper insight in the capabilities, limitations and requirements of test and the test flow. This will be done at first by situating simulation, verification and test in the product design, manufacturing and test flow. Next the role of Test and the different aspects that make up a test flow and a test program will be reviewed. Following that the different ways to test a circuit (test approaches) will be discussed from a methodological viewpoint as well as from a test parameter viewpoint. The methodological viewpoint will explore the path from Functional over Structural to Defect oriented test, thereby looking at the definition and application of fault models and how these can help to guide and improve the test process. The test parameter viewpoint will focus on the difference between voltage (logic) and current (IDDQ) testing and zoom in to IDDQ testing.
Having a proper insight in "What is Test all about and how can it be done" enables to built the bridge between Design and Test.

In the "Bridging Design and Test" section that bridges the Design and Test world, the design task that are done in function of test preparation will be looked at, leading to the discussion of topics like test vector generation, fault simulation and fault grading. Once these aspects are mastered, a second theme that will be

addressed is the difference between fault coverage and test coverage, putting meaning to the figures provided by the ATPG tools. Jumping back and forward between Design and Test the link will be made between "fault detection" and "defect detection", answering the question "how efficient are tests driven by fault models in detecting real life defects?". This will be elaborated further and underlined with practical data in the section "test quality and the quest for 0ppm" that will address fault coverage and test coverage requirements for a 0ppm goal. Looking at the relation between DPM figures and device reliability will conclude the "Bridging Design & Test" section.

The focus of the "Design perspective" section is to focus on the measures that can be taken during the design phase to ease and anticipate the test tasks. A well-selected design-for-test strategy is crucial to be able to meet quality and reliability targets as well as to anticipate test economic factors. Starting with defining what testability means, followed by an overview of the design-for-test basics and their impact on the design freedom, the question on "how to design a testable circuit" will be addressed. Answering this question will address themes like "Scan", "Boundary Scan" and "Built-in self Test (BIST)" and their application, as well as the "I_{DDQ} design for Test" requirements and implementation considerations.

Looking forward as well as compiling the gathered knowledge three approaches for mastering increasing amounts of test data in combination with test optimization without affecting test quality will be reviewed, followed by the discussion of a number of case studies and related test economics.

The training class is concluded by a set of global conclusion.

Upon completing this training class the participant will have acquired a proper understanding of the capabilities and limitations of Test as well as a proper understanding of the DFT measures that can be taken to improve the test process and reduce product costs. With this knowledge the participant will have the proper knowledge to take the appropriate decisions that help to bridge the gap between Design and Test and have a better understanding of the factors involved in reaching a 0ppm quality level.

Confidential

Tentative Training Class Timing

09.00 – 10.20: Part 1
Objectives, About Q-Star, 0ppm program, General Introduction, From Problem to Product.
(slides 1-26)
10.20 – 10.40: Break

10.40 – 12.00: Part 2
The role of Test, From Functional via Structural to Defect oriented Test, Structural test – the situation today
(slides 27-73)
12.00 – 13.30: Lunch break

13.30 – 14.50: Part 3
Test Approaches – voltage versus current test, Test vector generation, ATPG – fault coverage vs test coverage.
(slides 74-124)
14.50 – 15.10: Break

15.10 – 16.30: Part 4
Fault detection vs defect detection, Test Quality and the quest for 0ppm, DPM and reliability, Design for Test – intro, DFT – how to design a testable circuit.
(slides125- 182)
16.30 – 16.45: Break

16.45 – 18.00: Part 5
I_{DDQ} design for Test, Mastering test data, Case studies, Conclusions, Q&A.
(slides 183 – end)